EXPRESS MAIL LABEL NO. EL 862 486 584 US PATENT APPLICATION

UNITED STATES PATENT APPLICATION

of

JAMES R. EATON, JR.

and

MICHAEL C. FISCHER

for

ADDRESS STRUCTURE AND METHODS FOR MULTIPLE ARRAYS OF DATA STORAGE MEMORY

TO THE COMMISSIONER OF PATENTS AND TRADEMARKS:

Your petitioners, James R. Eaton, Jr., citizen of the United States, whose residence and postal mailing address is 373 Shasta Drive, Palo Alto, California 94306, and Michael C. Fischer, citizen of the United States, whose residence and postal mailing address is 763 East Charleston Road, Palo Alto, California 94306, pray that letters patent may be granted to them as the inventors of an **ADDRESS STRUCTURE AND METHODS FOR MULTIPLE ARRAYS OF DATA STORAGE MEMORY** as set forth in the following specification.

ADDRESS STRUCTURE AND METHODS FOR MULTIPLE ARRAYS OF DATA STORAGE MEMORY

FIELD OF THE INVENTION

The present invention pertains to the field of digital memory circuits. More particularly, this invention relates to address structures and methods for selecting a data memory storage cell in a data storage array within a matrix of data storage arrays on a single substrate.

BACKGROUND OF THE INVENTION

Many consumer devices are now constructed to generate and/or utilize digital data in increasingly large quantities. Portable digital cameras for still and/or moving pictures, for example, generate large amounts of digital data representing images. Each digital image may require up to several megabytes (MB) of data storage, and such storage must be available in the camera. To provide for this type of data storage application, the storage memory should be relatively low in cost for sufficient capacities of around 10 MB to hundreds of gigabytes (GB). The storage memory should also be low in power consumption, much less than one watt, and have relatively rugged physical characteristics to cope with the portable battery powered operating environment. For archival storage, data need only be written to the memory once. Preferably the memory should have a short access time (in the order of milliseconds) and moderate transfer rate (e.g. 20 Mb/s). Preferably, also, the storage memory should be able to be packaged in an industry standard interface module, such as PCMCIA or Compact Flash card.

One form of write-once compact information storage is shown in U.S. Patent No. 6,055,180, granted to Gudesen et al. on April 25, 2000, in which matrices of individually addressable cells are provided in layers between orthogonally arranged conductors. The cells may be comprised of cross-point diodes, OLEDs, bistable liquid crystal elements or other devices that change state with the introduction of heat and/or light.

Another application in portable devices for providing high density archival storage is described in co-pending United States Patent Application serial number 09/875,356, filed June 5, 2001 entitled "Non-Volatile Memory" (Hurst, et al), the disclosure of which is hereby incorporated herein by reference. The memory system disclosed therein, referred to as portable inexpensive rugged memory (PIRM), aims to

provide high capacity write-once memory at low cost for archival storage. This is realized in part by avoiding silicon substrates, minimizing process complexity and lowering areal density. The memory system includes a memory module formed of a laminated stack of integrated circuit layers constructed on plastic substrates. Each layer contains a cross-point diode memory array, and sensing of the data stored in the array is carried out from a separate integrated circuit remotely from the memory module.

Figures 1A and 1B show a typical PIRM memory structure on a substrate layer. The memory structure is comprised of a data storage array made up of a matrix of storage cell diodes at the intersections of row lines and column lines. Row and column decoder circuitry are connected to each of the row and column lines to address the selected storage cell diode. Row and column lines supply power to the data storage array.

In a further effort to compact data, multiple arrays are placed on a single substrate. Figure 3 shows a two-by-two matrix of four memory arrays on a substrate. Each array has its own matrix of storage cells with corresponding row and column lines. Row and column address lines are connected through appropriate decoder circuitry to the rows and columns of each array.

As used herein, "coplanar" means lying in the same plane. The term "coplanar conductor layer" refers to a conductor layer in a data storage device like a cross-point memory cell in which all conductors in the layer are arranged in the same plane. The terms "coplanar memory array," "coplanar memory device," "coplanar memory matrix" or "coplanar data storage cell" refer to a memory array, device, matrix or data storage cell that has multiple planes or layers of like elements, such as a coplanar row conductor layer, a coplanar column conductor layer and a coplanar diode layer. In coplanar memory devices and arrays, all row conductor lines extend without cross-over in one plane or layer and all column conductors extend without cross-over in another plane or layer.

A coplanar memory array may contain two layers of conductors, an upper layer and a lower layer. Memory cell diodes may lie in a third plane sandwiched between the upper and lower layers. Arbitrarily, we can say that all row conductors and other conductors running horizontally in the figures are on the lower layer of the array and all column conductors and other conductors running vertically in the figures are on the upper layer of the array. On each layer, the conductors are not allowed to

cross over one another, because such cross-overs would require additional difficult process steps, such as critically aligned vias. As used herein, the term "cross-over" refers to cross overs within an upper or lower layer, as described above.

The matrix of arrays shown in Figure 3 shows the limits of conventional coplanar memory design wherein each array has column and row lines at one of the four corners of the two-by-two matrix of arrays. Using the memory array structure shown, in order to build a more complex matrix of arrays by adding more arrays in some fashion, cross-over lines would be needed, thereby defeating the coplanar lithography and requiring much more complexity in memory design.

Another problem with the memory matrices shown in Figures 1 and 3 is the undesirable dissipation of power. In the array design shown, all decoder resistors draw current during operation, thereby dissipating much more power than desired. Moreover, all data cell diodes that are not on a selected row or column are strongly reverse biased by the address line voltages. This reverse bias voltage causes undesirable leakage currents to flow in the unselected data diodes. In an array of up to ten million diodes, even a very small leakage current per cell can result in large power dissipation. In addition to this power loss problem, the leakage current may be large enough to interfere with or obscure the sense currents indicating the values of the selected data cells.

Accordingly, a different memory matrix design is needed to enable additional memory arrays to be placed on a single substrate in a coplanar design. Moreover, address structure is needed that minimizes or eliminates power dissipation from unselected cells, because of decoder resistor current and leakage current from reverse biased cells.

SUMMARY OF THE INVENTION

The present invention comprises novel structures and methods for disposing multiple memory arrays on a single substrate while maintaining a coplanar design with no cross-over lines. The present invention further comprises a coplanar multiple memory matrix having minimal power dissipation from undesirable current in unselected decoder resistors or from leakage current in unselected data cells.

In one embodiment, an electrically addressable data storage unit has a plurality of data storage arrays, each array having a matrix of data storage cells connected by row lines and column lines for recording, addressing and reading of data. The storage unit has a plurality of row address lines, each row address line being in electrical

communication with the rows of predetermined multiple arrays of the plurality of data storage arrays. The data storage unit further has a plurality of column address lines, each column address line being in electrical communication with the columns of predetermined multiple arrays of the plurality of data storage arrays. A controller is connected to the plurality of row address lines and plurality of column address lines to selectively address a row of data storage cells in one of the multiple arrays and to selectively address a column of data storage cells in one of the multiple arrays, to thereby select a data storage cell in said one of the multiple arrays.

In another embodiment of the present invention, a method is provided for recording, addressing and reading of data in an electrically addressable data storage unit having a plurality of data storage arrays, each array having a matrix of data storage cells connected by row lines and column lines. A plurality of row and column address lines is provided for the plurality of arrays. Each row address line is in electrical communication with selected rows of multiple arrays to selectively address a row of data storage cells in one of the multiple arrays. Each column address line is in electrical communication with selected columns of multiple arrays to selectively address a column of data storage cells in one of the multiple arrays. A data storage cell in said one array is selectively addressed through a controller connected to the plurality of row address lines and plurality of column address lines.

Other aspects and advantages of the present invention will become apparent from the following detailed description, which in conjunction with the accompanying drawings illustrates by way of example the principles of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and **1B** are circuit diagrams of a typical prior art memory cell data storage array;

Figure 2 is another circuit diagram of a typical prior art memory cell data storage array;

Figure 3 is another prior art circuit diagram showing a matrix of memory cell data storage arrays;

Figure 4 is a circuit diagram of a matrix of memory cell data storage arrays according to an embodiment of the present invention;

Figure 5 is an enlarged partial circuit diagram of a portion of the matrix of memory cell data storage arrays of Figure 4 showing the line voltages for a read cycle, according to an embodiment of the present invention; and

Figure 6 is an enlarged partial circuit diagram of a portion of the matrix of memory cell data storage arrays of Figure 4 showing the line voltages for a write cycle, according to an embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Write-once or multiple rewrite memory circuits, storage systems, addressing and sensing circuits and methods for producing, implementing and using such circuits and systems are disclosed herein. In the following description, for purposes of explanation, specific nomenclature and specific implementation details are set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not necessarily required in order to practice the present invention.

In the following description, where "data" is referred to it will be appreciated that such "data" may be represented in various ways depending upon the context. As an example, "data" in a memory cell might be represented by a voltage level, a magnetic state, or a physical characteristic such as electrical resistance that presents a measurable effect such as voltage or current level or change to a sensing circuit, for instance. On the other hand, on a bus or during transmission such "data" might be in the form of an electrical current or voltage signal. Furthermore, herein "data" in most circumstances is primarily binary in nature which may for convenience be referred to as represented by states of "0" and "1", but it will be appreciated that the binary states in practice might be represented by relatively different voltages, currents, resistances or the like and it is generally immaterial whether a particular practical manifestation represents a "0" or a "1".

The present invention comprises structure and methods for multiple arrays of coplanar memory cells on a single substrate. An embodiment of this invention will be discussed in the context of a PIRM diode memory array of the type utilized in the memory system described in the above co-pending US patent application. In order to provide a thorough understanding of the invention, the following detailed description is therefore presented in the context of such a memory system, although those skilled in the art will recognize that the invention is not limited in application to the described structure.

PIRM Memory Structure

In order to understand the inventive aspects of the present invention, reference is first made to a typical PIRM diode memory structure 10 on a substrate 12, as shown

in Figure 1A. The memory structure 10 is comprised of a data storage array 14 made up of storage cell diodes 16 at the intersections of row lines 18 and column lines 20. A row decoder unit 22, comprised of row addressing (decoder) diodes 23 and row pull-up (decoder) resistors 24, is connected to each of the row lines 18 of the memory structure 10. Similarly, a column decoder unit 26, comprised of column addressing (decoder) diodes 27 and column pull-down (decoder) resistors 28 is connected to each of the column lines 20. Row address lines 30 and 31 are connected to each row line 18 through the row addressing diodes 23. Column address lines 32 and 33 are connected to each column 20 through the column addressing diodes 27. Sense line 34 provides an output-sensing signal during the read cycle. Row and column power lines 36 and 37, respectively, provide voltages to the data storage array 14. Row inhibit line 38 and column inhibit line 39 are utilized during the write cycle.

It should be understood that row address lines 30 and 31 and column address lines 32 and 33 are representative of the address lines necessary to provide all possibilities of address combinations to the memory array cells, so that each cell can be uniquely addressed. The actual number of row and column address lines necessary for a matrix of 6x6 cells as shown is easily determined by circuitry design theory. Only the two row and two column address lines are shown here that have row and column decoder diodes arranged so that cell 40 is addressed.

For example, as is well known in designing circuitry of the type shown, a three address bit diode decoder circuit requires three pair of positive-negative row address lines to address all output combinations. Each address line has four decoder diodes disposed in a different combination on eight output lines, so that all eight output states of the decoder can be selected and thereby select one of eight possible output lines.

In PIRM, a row decoder is used to select a row line as a decoder output line and a column decoder is used to select a column line as a decoder output line. Accordingly, different combinations of row and column address voltages enable access to a memory cell at the intersection of a selected row line and a selected column line.

The example shown herein assumes that row 1 goes positive and column 2 goes negative, thereby accessing cell 40. All of the address lines and decoder diode arrangements necessary to selectively access all cells in a given array are not shown here, because they are a simple matter of design to a person of ordinary skill in the art.

Likewise, power lines 36 and 37 are representative of all power lines to the memory array cells. The actual number of power lines will depend on the size and needs of the circuitry design. In the same manner, the row and column lines 18 and 20 are only representative of the number of lines in the memory array. Any number of row and column lines may be included, depending on the design of the memory array.

Figure 1B shows the line voltages in the circuitry structure in Figure 1A for the condition where memory cell 40 is being accessed. Row power line 36 is at +1 volts and column power line 37 is at –1 volt, thereby initially forward biasing all of the memory cells. The relevant row address lines 30 and 31 are set at –2 and +1 volts, respectively. The relevant column address lines 32 and 33 are set at +2 and –1 volts, respectively.

With the decoder diode arrangement shown, row address line 30 imposes –2 volts which is offset by the row power line +1 volt, so that all row lines except the row line of accessed memory cell 40 have a line voltage of –1 volt. Similarly, column address line 32 imposes a +2 volts on the column lines, which is offset by the –1 column power line supply voltage, resulting in a +1 voltage on each column except the column of the accessed cell 40. This arrangement reverse biases all of the memory cells except the accessed cell 40.

The row and column of cell 40 have row power supply voltage of +1 volt and a column power supply voltage of –1 volt, respectively, so cell 40 is the only cell with a voltage in a direction to forward bias the diode. Resistors R3 and R36 each have a voltage drop of 0.5 volts, so that the accessed memory cell has a +0.5 volts on row line 42 and –0.5 volts on column line 44. The voltage across the accessed cell 40 is 1 volt, (from +0.5 volts to –0.5 volts), the approximate voltage drop of the diode.

Summarizing, referring to the voltages applied in Figure 1B and to the character references in Figure 1A, during a read cycle in which memory cell 40 is selected, the following dynamics occur. The row power line 36 provides a positive voltage supply to the row pull-up resistors 24. The row address lines 30 provide the voltages to select the row lines that are to be pulled to a negative voltage by the currents that flow from the row power line 36 through the row pull-up resistors 24, the row addressing diodes 23 to the row address lines 30 that are at low voltage. Thus, a negative voltage is established on all row lines 18 except for row 42, which is powered to a positive voltage by row power line 36.

Similarly, the column power line 37 provides a negative voltage to the column pull-down resistors 28. The column address lines 32 provide the voltages to select the column lines 20 that are to be pulled to a positive voltage by the currents that flow from the column address lines 32, through the column addressing diodes 27, the pull-down resistors 28 to the column power line 37. Thus, a positive voltage is established on all column lines 20 except one column line 44, which is powered to a negative voltage by the column power line 37.

The selected memory cell 40 is at the intersection of row line 42 and column line 44. The voltage direction causes forward current flow in the selected memory cell diode. In the event that the diode is conducting (a one state), current flows to diode 40 from the row power line 36 through the row pull-up resistor R3 on row line 42, through the selected memory cell diode 40, through the pull-down resistor R36 in column line 44 to the column power line 37. If the diode is blown and is not conducting (a zero state), the current flows through the row pull-up resistor R3 on the selected row 42 to the sense line 34. The absence or presence of current on sense line 34 is sensed externally to determine the one or zero state of the accessed memory cell diode 40.

During a write cycle, if the state of selected memory cell 40 is to be changed from a one state to a zero state, the voltages on the row and power supply lines 36 and 37 and on the row and column address lines 30 and 32 are increased to the point that the addressed cell 40 experiences a voltage stress sufficient to change the state of the diode. Since many layers of memory units 14 may be stacked on multiple substrates, the same cell is selected on each of the many layers, thereby enabling writing of multiple bits simultaneously.

To accomplish writing of data, the voltages of the row and column inhibit lines 38 and 39, respectively, are set to voltages near ground to shield the selected cell diode from experiencing the voltage stress and thereby inhibiting writing. In some design embodiments, a second sense line may be added to the column circuitry. For this simple array, the sense lines could double as inhibit lines. In the following figures, the inhibit lines may be separate from the sense lines.

One of the advantages of the foregoing memory array is that the memory array structure is all coplanar, that is, the conductor elements are laid out with a row conductor layer in one plane and a column conductor layer in another plane, all contacting the memory cells directly without the necessity of any cross-over of

conductors within each conductor layer. Since the row lines are disposed within a top conductor layer and the column lines are disposed within a bottom layer, there is no need for cross-over of the conductors within either conductor layer.

PIRM Memory Structure With Power Striping

Two power dissipation problems occur with the foregoing memory cell structure. First, during operation, all of the pull-up and pull-down resistors 24 and 28 (Fig. 1A) are drawing current, thereby undesirably dissipating power. Second, all data diodes 16 not on a selected row or column are strongly reverse biased by the voltages on the row and column address lines 30 and 32 through the row and column decoder diodes 23 and 27. This reverse bias voltage causes undesirable leakage currents to flow in the data diodes 16. Although each leakage current is small, the sum over an array of ten million diodes can result in large power dissipation as well as interfering with and obscuring the output data on the sense lines.

In Figure 2, a modification called power striping is provided to reduce the first power dissipation problem. The row power line 36 is replaced by three row power lines 50, 52 and 54, each directed to a different segment of the row decoder unit 22. Row power line 50 is connected to row decoder resistors R3 and R4. Row power line 52 is connected to row decoder resistors R17 and R18, and row power line 54 is connected to row decoder resistors R37 and R38.

Similarly, the column power line 37 is replaced by three column power lines 60, 62 and 64, each directed to a different segment of the column decoder unit 26. Column power line 60 is connected to column decoder resistors R35 and R36. Column power line 62 is connected to column decoder resistors R31 and R32, and column power line 64 is connected to column decoder resistors R27 and R28.

This structure enables power to be supplied only on row power line 50 and column power line 60, so that power is provided only to the four memory diodes in a segment 66 of the memory array 14 in which the selected memory cell 40 is located. This approach substantially reduces the first power dissipation problem by only drawing current through those portions of the row and column decoders required to address a relatively small segment of the memory matrix. Unfortunately, this structure does not address the second power dissipation problem of substantial power loss through reverse biasing the memory cells.

PIRM Memory Structure in Two-By-Two Memory Matrix

Referring now to Figure 3, a memory structure 70 is shown in which the memory structure shown in Figure 1 is duplicated to provide four memory arrays 72, 74, 76, 78 on a single substrate 71 in a two-by-two matrix. The structure shown in Figure 1 is repeated with geometric flip and rotation so that all control and sense lines are located at different corners of memory structure 70 and extend unbroken and without cross-over to be accessed by input and output pins outside of the memory structure 70. Each memory array is electrically independent of the other memory arrays. The arrays can be operated simultaneously, with decoder resistors drawing current and memory cell diodes providing reverse leakage currents simultaneously. Alternatively, the arrays that do not have selected cells can be depowered to reduce resistor and memory cell power dissipation.

The matrix structure shown in Figure 3 retains most of the layout regularity and is coplanar, as described above. However, no further memory arrays can be added to the matrix, if it is to remain coplanar with no conductor cross-overs within conductor layers. All four corners of the two-by-two matrix are utilized with power, address and control lines, so any addition arrays would require a cross-over or segmented layout for its power, control and address lines to have access to an outside controller and power supplies. Thus, the coplanar layout described is limited to four memory arrays on a substrate.

Coplanar Matrix of Memory Storage Arrays – Overview

The foregoing description has provided the context for the present invention. Several embodiments of the present invention shall now be described below. It is understood that other embodiments of the present invention may be described and shall fall within the scope of the appended claims.

Referring first to Figure 4, a three-by-three memory array matrix 80 is shown, according to the present invention. In this structure, a matrix of nine memory arrays 81-89 is arranged on a single substrate 90. The power, control and address lines are arranged in a novel and inventive manner to enable a coplanar matrix layout. Using the structure of the current invention, more complex matrices with even more memory arrays may be arranged on a single substrate. Hence the present invention represents a substantial break-through in coplanar memory technology that will enable substantially more compact coplanar memory layouts.

The key to this new structure is the implementation of unbroken address lines that extend across multiple arrays along the entire length or width of the matrix. Thus, row address lines 91 and 92 are connected to and extend through the row decoder circuitries of arrays 87, 84 and 81. Likewise, row address lines 93 and 94 are connected to and extend through the row decoder circuitries of arrays 88, 85 and 82. Row address lines 95 and 96 are connected to and extend through the row decoder circuitries of arrays 89, 86 and 83. Each row address line is connected to the row decoder circuitries of each array in the same manner shown in Figures 1-3.

Similarly, column address lines 97 and 98 are connected to and extend through the column decoder circuitries of arrays 87, 88 and 98. Column address lines 99 and 100 are connected to and extend through the column decoder circuitries of arrays 84, 85 and 86. Column address lines 101 and 102 are connected to and extend through the column decoder circuitries of arrays 81, 82 and 83. Each column address line is connected to the column decoder circuitry of each array in the same manner shown in Figures 1-3.

There is a separate power supply line for each array, so that each array is individually turned on or off, depending on whether the array is selected. Thus, row power supply lines 104, 105 and 106 are separately connected to the row decoder resistors 81a, 84a and 87a, respectively. Similarly, row power supply lines 107, 108 and 109 are separately connected to the row decoder resistors 82a, 85a and 88a, respectively. Row power supply lines 110, 111, and 112 are separately connected to the row decoder resistors 83a, 86a and 89a, respectively. Each row power supply line is connected to its corresponding row decoder resistors in the same manner shown in Figures 1-3.

Similarly, column power supply lines 114, 115 and 116 are separately connected to the column decoder resistors 81b, 82b and 83b, respectively. Likewise, column power supply lines 117, 118 and 119 are separately connected to the column decoder resistors 84b, 85b and 86b, respectively. Column power supply lines 120, 121 and 122 are separately connected to column decoder resistors 87b, 88b and 89b, respectively.

There is a separate sense line for each array, enabling each array to be individually sensed, depending on whether the array is selected. Thus, sense lines 124, 125 and 126 are separately connected to arrays 87, 84 and 81, respectively. Sense lines 127, 128 and 129 are separately connected to arrays 88, 85 and 82,

respectively. Sense lines 130, 131 and 132 are separately connected to arrays 89, 86 and 83, respectively. Alternately, the sense lines may be connected together along each column without interfering with the operation of the arrays. However, with only one sense line the line voltages will not be matched and there will be some leakage current.

A single row inhibit line is connected to and extends through the row decoder circuitries of all arrays in a given column. Thus, row inhibit line 134 is connected to and extends through the row decoder circuitries of arrays 87, 84 and 81. Row inhibit line 135 is connected to and extends through the row decoder circuitries of arrays 88, 85 and 82. Row inhibit line 136 is connected to and extends through the row decoder circuitries of arrays 89, 86 and 83.

In contrast, separate column inhibit lines are independently connected to the column decoder circuitries of each array. Thus, column inhibit lines 138, 139 and 140 are separately connected to the column decoder circuitry of arrays 81, 82 and 83, respectively. Column inhibit lines 141, 142 and 143 are separately connected to the column decoder circuitry of arrays 84, 85 and 86, respectively. Column inhibit lines 144, 145 and 146 are separately connected to the decoder circuitry of arrays 87, 88 and 89, respectively. This arrangement simply shows that separate inhibit lines can be connected to each array in a row with different voltages on each inhibit line. This structure makes it possible to match the voltages on unselected arrays more closely, thereby reducing leakage current from the arrangement where there is only one inhibit line per column or per row.

The foregoing structure and connections of the matrix of three-by-three memory arrays provides the ability to simultaneously read a word of data from a stack of memory layers on separate substrates, each of which sees the same applied address voltages and power supply voltages. With this structure, as many arrays as desired can be placed on a layer, according to specific design needs. The selection of voltage levels on the power supply lines to match the address voltages and sense and inhibit lines provides equal voltages on the row and address lines of unselected arrays, thereby turning off the unselected arrays. Thus, undesirable leakage currents in data diodes of unselected arrays are eliminated.

Coplanar Matrix of Memory Storage Arrays – Read Cycle

Referring now to Figure 5, the line voltages are given for a read cycle in which a memory cell 150 is read in the lower left array 87. In Figure 5, only array 87 and

immediately adjacent arrays 84, 85 and 88 are shown, so the line voltages can be seen more clearly. Array 81 is an unselected array in the column of array 87, so it has the same line voltages as array 84. Array 89 is an unselected array in the row of array 87, so it has the same line voltages as array 88. Array 85 is not in a row or column with array 87 and is entirely turned off, as are arrays 82, 83 and 86 (not shown).

The cells in array 87 are powered with +1 volts on row power line 1 and −1 volts on column power line 1. The selected cell 150 is forward biased with +1 volts on row address line 92 and −1 volts on column address line 98. All other diode cells in array 87 are reversed biased, with -2 volts on row address line 91 and +2 volts on column address line 97.

The state of cell 150 is observed by sensing the lack or presence of a current in the sense line 124 that is connected to the decoder row lines. Sense line 1 is set at 0 volts to enable a current flow, since the row of the desired cell 150 is positive. The other sense lines 2 and 3 are set at −2 volts to match the −2 voltage on the rows of the other arrays 81 and 84 in the same column as array 87, thereby matching that voltage to minimize leakage current through the unselected sense lines.

Row inhibit line 134 is set at +1 to take it out of operation, since that voltage is higher than any of the row voltages in array 87. Similarly, column inhibit line 1 is set at −1 to take it out of operation during the read cycle. The other column inhibit lines 2 and 3 go to the other arrays 88 and 89 in the same row as array 87. They are set at +2 to match the column voltages in the arrays 88 and 89, thereby eliminating any leakage current through those two inhibit lines.

The row address voltages applied to row address lines 91 and 92 are carried to all other arrays in the same column, namely arrays 81 and 84. Likewise, the column address voltages applied to column address lines 97 and 98 are carried to all other arrays in the same row, namely arrays 88 and 89. In order to shut off these unselected arrays, the voltages on the power lines are adjusted. Thus, the row power lines, row address lines and row inhibit lines of the unselected arrays 88 and 89 are all set at +2. Similarly, the column power lines, the column address lines and the column inhibit lines of the unselected arrays 81 and 84 are all set at −2. In this manner, the row voltages and column voltages are matching, depending on the address voltages provided to each array. This matching of row and line voltages shuts off the memory cells in unselected arrays 81, 84, 88 and 89.

The cells that are not in the row or column of array 87 having the selected cell 150, namely arrays 82, 83, 85 and 86, are turned off by simply setting the row and column power lines to zero. Using this approach, the data diodes in all of the unselected arrays have zero applied voltage, thereby eliminating leakage currents. Note that this structure is powered from only two sides. It may be duplicated, mirrored and/or flipped as discussed earlier, as needed for external connections and other design requirements.

Figure 5 shows the line voltages for a portion of the circuitry structure in Figure 4 for the condition where memory cell 150 is being read. Looking first at array 87, row power line 1 is at +1 volts and column power line 1 is at –1 volt, thereby initially forward biasing all of the memory cells. The relevant row address lines 91 and 92 are at –2 and +1 volts, respectively. The relevant column address lines 97 and 98 are at +2 and –1 volts, respectively.

The line voltages are the same for array 87 as they are for array 10 in Figure 1B. With the decoder diode arrangement shown, all row lines except the row line of accessed memory cell 40 have a line voltage of –1 volt. Similarly, all column lines have a +1 voltage on each column except the column of the accessed cell 150. This arrangement reverse biases all of the memory cells except the accessed cell 150.

The row and column of cell 150 have +0.5 volts and –0.5 volts, respectively, so that cell 150 is the only cell with a voltage in a direction to forward bias the diode. Resistors R3 and R36 each have a voltage drop of 0.5 volts, so that the accessed memory cell has a +0.5 volts on the row line for cell 150 and –0.5 volts on the column line for cell 150. The voltage across the accessed cell 1500 is 1 volt, (from +0.5 volts to –0.5 volts), the approximate voltage drop of the diode.

Looking now at array 84 in Figure 5, the row power 2 is set at –2 volts. The column power line 1 for array 84 is also at –2 volts, so the voltage on either side of the memory cells in array 84 are matched and the cells are off, without being reversed biased. As shown, the column and row line voltages for array 84 are all –2 volts. Array 81, not shown, has the same voltage arrangement.

Similarly, array 88 has row power 1 set at +2 volts, and the column power 2 is set at +2 volts. Accordingly, the row lines and column lines of array 88 are all set at +2 volts and all of the cells are turned off without being reverse biased. Array 89, not shown, has the same voltage arrangement.

Coplanar Matrix of Memory Storage Arrays – Write Cycle

Referring now to Figure 6, the line voltages are given for a write cycle in which a memory cell 150 is written in the lower left array 87. Similar to Figure 5, in Figure 6 only arrays 87, 84, 85 and 88 are shown, so the line voltages can be seen more clearly. Array 81 is an unselected array in the column of array 87, so it has the same line voltages as array 84. Array 89 is an unselected array in the row of array 87, so it has the same line voltages as array 88. Array 85 is not in a row or column with array 87 and is entirely turned off, as are arrays 82, 83 and 86 (not shown).

In the write operation, all voltages are increased to provide a larger voltage stress across the accessed cell 150. Thus, the cells in array 87 are powered with a +2 voltage on row power line 106 and a –2 voltage on column power line 120. The interrogated cell 150 is forward biased with a +2 voltage on row address line 92 and a -2 voltage on column address line 98. All other diode cells in array 87 are reversed biased, with a -3 voltage on the row address line 93 and a +3 voltage on the column address line 97. The row inhibit line 134 of array 87 is set at +2. The column inhibit line 122 for array 87 is at –2. The state of cell 150 is observed by sensing the lack or presence of a current in the sense line 124 that is connected to the decoder row lines.

To shut off the other arrays in the row and column of array 87, namely arrays 81, 84, 88 and 89, the row power lines, row address lines and row inhibit lines of the unselected arrays 88 and 89 are all set at +3. Similarly, the column power lines, column address lines and column inhibit lines of the unselected arrays 81 and 84 are set at –3. As in the read cycle, the cells that are not in the row or column of array 87 having the selected cell 150, namely arrays 82, 83, 85 and 86, are turned off by simply setting the row and column power lines to zero.

Coplanar Matrix of Memory Storage Arrays – Write Inhibit Cycle

Referring again to Figure 6, if it is desired to inhibit the write to memory cell 150, the voltage on the row inhibit line 134 is changed from +2 to –1 and the voltage on the column inhibit line is changed from -2 to +1. This causes the row and column decoders to zero bias the accessed cell 150 and prevent application of the voltage stress. This inhibit function enables the writing of data on multiple memory layers, each of which have the same address and power supply voltages, but have unique inhibit signals.

It can be seen from the foregoing description that the present invention provides several advantages over prior memory arrays. The present structure provides

a memory matrix design that enables additional memory arrays to be placed on a single substrate in a coplanar design. Almost any number of multiple memory arrays may be disposed on a single substrate while maintaining a coplanar design with no cross-over lines. The present invention further comprises a coplanar multiple memory matrix in which the row and column voltages of unselected arrays are equal, thereby providing no reverse or forward bias on the diodes in the unselected arrays. This approach results in minimal power dissipation from undesirable current in unselected decoder resistors or from leakage current in unselected data cells.

It is understood that the number of row and column address lines may change as a function of the number of memory cells in a given array. Also the number of row and column power lines may vary in relation to the number of arrays in a respective row or column of the matrix of arrays. As stated before, the sense lines or the inhibit lines can be dedicated for each array or can serve multiple arrays in a given column or row. In the latter case, the voltages in all of the unselected cells may not be matched, so that reverse biasing may occur, resulting in some leakage current. In addition, power striping may be included for some or all of the arrays, minimizing the amount of unnecessary current through the decoder resistors.

The principles of the present invention can be applied with many other variations to the circuits, structures, arrangements and processes described herein, as will be apparent to those of ordinary skill in the art, without departing from the scope of the invention as defined in the appended claims.